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EXAMINER
DAY, HERNG DER

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ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/802,787	KHANNA ET AL.
	Examiner	Art Unit
	Herng-der Day	2128

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined and claims 1-24 have been rejected.

Drawings

2. The drawings are objected to for the following reasons.

2-1. In FIG. 1, it appears that the reference character "26" of "PCI/LEGACY BRIDGE" should be "28" and the reference character "28" of "LEGACY BUS" should be "26".

2-2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

(a) block 72, as described in line 13 of page 10.

2-3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "70" has been used to designate both "Attach another GRB GUID to Handle" in FIG. 4 and "Handle" example in FIG. 5A.

2-4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

Appropriate correction is required.

3-1. As described in lines 9-10 of page 8, "many PCI busses are controlled by an Intel [please provide an Intel chipset for a PCI bus] chipset." (Emphasis added).

3-2. It appears that "a point to the GRB is attached", as described in line 6 of page 10, should be "a pointer to the GRB is attached".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 19-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5-1. Claim 19 recites the limitation "the root bus" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5-2. Claim 21 recites the limitation "the object oriented representation" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5-3. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-18 are rejected under 35 U.S.C. 101 because the inventions as disclosed in claims are directed to non-statutory subject matter.

7-1. Claims 1-18 are not tangibly embodied because it could be practiced with pencil and paper. It is not in the technology arts.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furner et al., U.S. Patent 5,974,474 issued October 26, 1999, in view of Dinallo, U.S. Patent 5,727,212 issued March 10, 1998.

9-1. Regarding claim 1, Furner et al. disclose a method for representing a root bus, comprising:

creating a globally unique identifier (GUID) for the root bus (bus tag 134, FIG. 1B). Furner et al. also disclose peripheral buses are characterized by being connected, directly or indirectly, to the CPU-memory bus through bus controllers that actively manage the communication to the hardware devices on the bus (column 10, lines 13-16). Furthermore, Furner et al. disclose an installation information table as shown in FIG. 2E, which implies registering functions. However, Furner et al. fail to expressly disclose defining an object-oriented abstraction including methods. Nevertheless, Furner et al. do suggest the abstracting into functional modules. Thus, applications could refer to hardware instances in a common manner (column 31, lines 41-51).

Dinallo discloses bridging communications between an object oriented component and a procedural programmed device driver (Dinallo, column 2, lines 4-16). As shown in Fig. 3, Object includes multiple methods to provide different functions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Furner et al. to incorporate the teachings of Dinallo to obtain the invention as specified in claim 1 because by bridging communications between an object oriented component and a procedural programmed device driver the existing procedural programmed device driver could be reused in the OOP environment.

9-2. Regarding claim 2, Furner et al. further disclose the object-oriented abstraction comprises one of a C++ object or Java object (C++, column 31, lines 41-45).

9-3. Regarding claim 3, Furner et al. further disclose the root bus comprises a PCI bus (primary bus, PCI, column 10, lines 40-42).

9-4. Regarding claim 4, Furner et al. further disclose comprising enumerating the root bus and said any subordinate busses through use of the methods that are registered (retrieved information, column 13, lines 22-28).

9-5. Regarding claim 5, Furner et al. further disclose the set of components of the object-oriented abstraction include at least one variable for storing information, further comprising storing configuration information derived during enumeration of the root bus into said at least one variable (reference table, column 13, lines 22-28).

9-6. Regarding claim 6, Furner et al. further disclose comprising allocating resources for the root bus, each subordinate bus, and any devices attached to those root and subordinate busses (resource setting 142, column 12, lines 39-47); and

storing information corresponding to resources that are allocated in said at least one variable for storing information (storing information, column 13, lines 22-28).

9-7. Regarding claim 7, Furner et al. further disclose functions of the root bus are controlled, at least in part, by a chipset having a plug-in driver, further comprising interrogating the plug-in driver to identify said plurality of methods (bus controllers, column 10, lines 28-30).

9-8. Regarding claim 8, Furner et al. further disclose functions of the root bus are controlled, at least in part, by a chipset having a plug-in driver, further comprising publishing the object-oriented abstraction via the plug-in driver (run-time memory 101, FIG. 1B).

9-9. Regarding claim 9, Furner et al. disclose a method for defining resource configuration information in a system that includes a plurality of root busses, comprising:

identifying each of the plurality of root busses (primary buses, column 10, lines 10-16);

assigning a bus identifier for each of the subordinate busses (bus tag 134, FIG. 1B).

Furner et al. also disclose peripheral buses are characterized by being connected, directly or indirectly, to the CPU-memory bus through bus controllers that actively manage the communication to the hardware devices on the bus (column 10, lines 13-16). Furthermore, Furner et al. disclose an installation information table as shown in FIG. 2E, which implies registering functions. However, Furner et al. fail to expressly disclose defining an object-oriented abstraction of each root bus including methods. Nevertheless, Furner et al. do suggest the abstracting into functional modules. Thus, applications could refer to hardware instances in a common manner (column 31, lines 41-51).

Dinallo discloses bridging communications between an object oriented component and a procedural programmed device driver (Dinallo, column 2, lines 4-16). As shown in Fig. 3, each Object includes multiple methods to provide different functions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Furner et al. to incorporate the teachings of Dinallo to obtain the invention as specified in claim 1 because by bridging communications between an object oriented component and a procedural programmed device driver the existing procedural programmed device driver could be reused in the OOP environment.

9-10. Regarding claim 10, Furner et al. further disclose the object oriented representation includes a globally unique identifier (GUID) for each root bus (bus tag 134, FIG. 1B).

9-11. Regarding claim 11, Furner et al. further disclose comprising:

creating a handle (run-time memory 101, FIG. 1B); and

storing references corresponding to the GUIDs for each root bus in the handle (reference table, column 13, lines 22-28).

9-12. Regarding claim 12, Furner et al. further disclose the handle further includes indicia for each GUID identifying a location of the object oriented representation corresponding to the GUID (driver location 208, FIG. 2B).

9-13. Regarding claim 13, Furner et al. further disclose comprises a pointer to the memory address at which the object oriented representation is stored (reference table, column 13, lines 22-28).

9-14. Regarding claim 14, Furner et al. further disclose each root bus and any subordinate busses connected either directly or indirectly to the root bus form a hierarchy, and wherein the enumeration process for each root bus comprises:

assigning bus identifiers as subordinate busses are reached while moving downward through the hierarchy (bus tag 134, FIG. 1B); and

calculating resource requirements for each subordinate bus while moving back up the hierarchy (calculated information, column 13, lines 22-28).

9-15. Regarding claim 15, Furner et al. further disclose comprising:

determining resource requirements for each subordinate bus (resource setting 142, FIG. 1B);

allocating the resource requirements for that subordinate bus (resource setting 142, FIG. 2E); and

setting resources for that subordinate bus (allocate system resources, column 12, lines 39-47).

9-16. Regarding claim 16, Furner et al. further disclose at least one of the subordinate busses for a given root bus has a peripheral device connected to it, and further wherein determining the resource requirements for each subordinate bus includes determining the resource requirements of any peripheral devices attached to that subordinate bus (hardware devices 148, FIG. 1B).

9-17. Regarding claim 17, Furner et al. further disclose comprising:

allocating resources for each root bus based in part on the resources of its subordinate busses (resource setting 142, FIG. 1B); and

setting the resources for that root bus (allocate system resources, column 12, lines 39-47).

9-18. Regarding claim 18, Furner et al. further disclose comprising:

evaluating devices in the hierarchy of each root bus to determine if they produce a firmware device or an optional ROM that may include BIOS corresponding to a bootable device (compares the information in each drive record with that in the hardware device records, column 15, lines 8-18).

9-19. Regarding claim 19, this article of manufacture claim includes same method limitations as in claim 1 and is unpatentable using the same analysis of claim 1.

9-20. Regarding claim 20, Furner et al. further disclose the computer- executable instructions comprises one or more software modules including a root bus driver (drivers 121, FIG. 1B).

9-21. Regarding claim 21, Furner et al. further disclose execution of the instructions further performs the function of assigning a bus identifier for each of the subordinate busses through use

of an enumeration process that implements one or more of the methods referenced by the object oriented representation of that root bus (bus tag 134, FIG. 1B).

9-22. Regarding claim 22, Furner et al. further disclose the root bus and any subordinate busses connected either directly or indirectly to the root bus form a hierarchy, and wherein the enumeration process for the root bus comprises:

assigning bus identifiers as subordinate busses are reached while moving downward through the hierarchy (bus tag 134, FIG. 1B); and

calculating resource requirements for each subordinate bus while moving back up the hierarchy (calculated information, column 13, lines 22-28).

9-23. Regarding claim 23, Furner et al. further disclose execution of the instructions further performs the functions of:

determining resource requirements for each subordinate bus (resource setting 142, FIG. 1B);

allocating the resource requirements for that subordinate bus (resource setting 142, FIG. 2E); and

assigning the resources that are allocated to the root bus that is a parent of that subordinate bus (allocate system resources, column 12, lines 39-47).

9-24. Regarding claim 24, Furner et al. further disclose execution of the instructions further performs the functions of:

creating a handle (run-time memory 101, FIG. 1B); and

storing references corresponding to a GUID for the object-oriented abstraction and a pointer to the object-oriented abstraction in the handle (reference table, column 13, lines 22-28).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Lin et al, U.S. Patent 6,421,798 B1 issued July 16, 2002, and filed July 14, 1999, is cited as disclosing a chipset-based memory testing method.

Reference to Hinson et al, U.S. Patent 6,748,455 B1 issued June 8, 2004, and filed February 23, 1999, is cited as disclosing an object-based event communications system.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean R. Homere can be reached on (571) 272-3780. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
December 13, 2004

JEAN R. HOMERE
PRIMARY EXAMINER